EE 2.3: Semiconductor Modelling in SPICE
Course homepage:  
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BJT Ebers-Moll Model and SPICE MOSFET model

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Summary of last lecture

We saw that:

- The SPICE diode model is a piecewise non-linear function, which includes breakdown

- It is essential to have the GMIN convergence aid in that model because the conductance of the diode is set to zero for much of the characteristic in reverse bias

- The exponential equation you know for the behaviour of a BJT is not accurate in the saturation region and so not useful (on its own) for a SPICE model

- The started to look at the development of the Ebers Moll BJT model

- We can think of the currents in a saturated BJT as being a sum of forward and reverse carrier flows in the base for equivalent forward and reverse BJTs operating in active mode
This lecture

- We will finish the Ebers-Moll model and see how it relates to the SPICE model
- We will look briefly at the SPICE MOSFET models
Reminder from last time - the BJT in saturation

Now let’s look at what happens to the device saturation. In saturation, both junctions are forward biased. If we look at the concentration of electrons in the device, we have:

![Figure 1 BJT electron concentration in saturation](image_url)
Carrier flows in Saturation...

- Electron current decreased
- Base current increased – holes injected into collector and emitter
Look at the electron current…

Can think of this as being made of a forward and a reverse flow of electrons (device in saturation in each case), due to the principle of linear superposition:

\[
I_t = K \frac{n_{pe}' - n_{pc}'}{L_b}
\]

\[
I_f = K \frac{n_{pe}'}{L_b}
\]

\[
I_r = K \frac{n_{pc}'}{L_b}
\]

\[
I_t = I_f - I_r = K \frac{n_{pe}' - n_{pc}'}{L_b}
\]

Where \( K \) is just a constant of proportionality and \( L_b \) is the length of the base
Carrier flows with forward and reverse currents

- Collection of electrons by emitter
- Normal injection at b-e junction
- Recombination in base
- Collection of electrons by collector
- Normal injection at b-c junction

Electron current

Hole current
Convert these carrier flows into a circuit diagram...

\[ I_F = I_{Nbe} + I_{Pbe} \]

\[ I_B = I_{Nbc} + I_{Pbc} \]

\[ B_R \times I_{Nbc} \]

\[ B_F \times I_{Nbe} \]

We are almost at the Ebers-Moll model…
We had already proved that in saturation:

$$\alpha_F I_F = B_F I_{Nbe}$$

And therefore we can also write:

$$\alpha_R I_R = B_R I_{Nbe}$$

This gives us the final well known Ebers-Moll injection model…
Ebers-Moll Injection Model

\[ I_F = I_{ES} \left[ \exp \left( \frac{V_{BE}}{nV_t} \right) - 1 \right] \]

\[ I_R = I_{CS} \left[ \exp \left( \frac{V_{BC}}{nV_t} \right) - 1 \right] \]
Ebers-Moll Equations

\[ I_C = \alpha_F I_F - I_R = \alpha_F I_{ES} \left[ \exp \left( \frac{V_{BE}}{nV_t} \right) - 1 \right] - I_{CS} \left[ \exp \left( \frac{V_{BC}}{nV_t} \right) - 1 \right] \]

\[ I_E = \alpha_R I_R - I_F = \alpha_R I_{CS} \left[ \exp \left( \frac{V_{BC}}{nV_t} \right) - 1 \right] - I_{ES} \left[ \exp \left( \frac{V_{BE}}{nV_t} \right) - 1 \right] \]

\[ I_B = -I_E - I_C = (1 - \alpha_F I_F) + (1 - \alpha_R I_R) \]

It appears we need 4 parameters to completely specify the model:

\[ I_{ES}, I_{CS}, \alpha_R, \alpha_F. \]
Simplify the model…

It can be shown that:

\[ \alpha_F I_{ES} = \alpha_R I_{CS} \]

(See the original paper by Ebers and Moll – “Large-Signal behaviour of junction transistors”).

We know in active mode:

\[ I_c = I_s \left[ \exp\left(\frac{V_{be}}{V_t}\right) - 1 \right] \]

Thus we can write:

\[ \alpha_F I_{ES} = \alpha_R I_{CS} = I_s \]
Apart from the fact that SPICE can use the existing diode models and existing current source models to make a BJT with the Ebers-Moll model, what is so great about the Ebers-Moll model for computer simulation?
It works under all operating conditions – active, saturation etc. SPICE does not need to implement different equations for different regions of operation.
1.1.1. Ebers-Moll Transport Model used in SPICE

SPICE does not use the injection model – it uses the transport model.

This is simply a change of notation…

\[ I_{CC} = I_S \left[ \exp\left(\frac{V_{BE}}{nV_t}\right) - 1 \right] \]

\[ I_{EC} = I_S \left[ \exp\left(\frac{V_{BC}}{nV_t}\right) - 1 \right] \]
One final change to get to the final model that SPICE uses…

Whilst the internal operation of the model is different, the terminal currents are the same for given terminal voltages….
What are physical meanings of $\beta_F$ and $\beta_R$?
• $\beta_F$ is the current gain ($I_C/I_B$) of the device when it is operating with the emitter as the emitter and the collector as the collector in the active mode

• $\beta_R$ is the current gain of the device when it is operating with the emitter as a collector and the collector as an emitter in the reverse active mode

Note that as the device is made to have higher forward current gain (the terminals for emitter and collector are not completely interchangeable due to different dopings of the collector and emitter) than reverse current gain.
Final DC static model

Add terminal resistances and the GMIN convergence aid conductances:
The important DC model SPICE parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IS ($I_s$)</td>
<td>The transistor saturation current</td>
</tr>
<tr>
<td>RE ($r_e$)</td>
<td>The Ohmic resistance of the contact and bond wire at the emitter</td>
</tr>
<tr>
<td>RB ($r_b$)</td>
<td>The Ohmic resistance of the contact and bond wire at the base</td>
</tr>
<tr>
<td>RC ($r_c$)</td>
<td>The Ohmic resistance of the contact and bond wire at the collector</td>
</tr>
<tr>
<td>NF ($n$)</td>
<td>The emission (or ideality) coefficient for the base-emitter junction</td>
</tr>
<tr>
<td>NR ($n$)</td>
<td>The emission (or ideality) coefficient for the base-collector junction</td>
</tr>
<tr>
<td>BF ($\beta_F$)</td>
<td>The forward current gain</td>
</tr>
<tr>
<td>BR ($\beta_R$)</td>
<td>The reverse current gain</td>
</tr>
</tbody>
</table>

Note that the BJT diode equations do not model breakdown, hence there are no BV and IBV parameters for the BJT model.
Large Signal Transient Model
Add in the capacitances of the two diodes:
Additional parameters to specify the transient model

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CJE</td>
<td>Zero bias base-emitter junction capacitance</td>
</tr>
<tr>
<td>CJC</td>
<td>Zero bias base-collector junction capacitance</td>
</tr>
<tr>
<td>VJE</td>
<td>Base-emitter junction built in voltage</td>
</tr>
<tr>
<td>VJC</td>
<td>Base-collector junction built in voltage</td>
</tr>
<tr>
<td>TF</td>
<td>Forward transit time</td>
</tr>
<tr>
<td>TR</td>
<td>Reverse transit time</td>
</tr>
</tbody>
</table>

There is also an area scaling parameter $A$ for the BJT, which works in exactly the same way as for the diode.
The SPICE MOSFET Models

DC Model

- Essentially 1 diode model used in SPICE and 1 BJT model
- Many MOSFET models
- We will look at the original ones available in PSpice
- BSIM (Berkeley Short Channel IGFET model) model. (Over 100 parameters in the DC model alone!)
The basic SPICE level 1 static model (as proposed by Shichman and Hodges) is as follows:

\[ I_{DS} = \mu_0 C_{ox} \frac{W}{L_{eff}} \left[ (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

\[ I_{DSsat} = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 \]
You are already familiar with an empirical correction to these equations to account for the channel length modulation:

\[
I_{DS} = \mu_0 C_{ox} \frac{W}{L_{eff}} \left[ (V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2} \right] \left[ 1 + \lambda V_{DS} \right]
\]

And:

\[
I_{DS_{sat}} = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 \left[ 1 + \lambda V_{DS} \right]
\]

These are the essentially the equations implemented by SPICE in the static model, but there are some points worthy of noting.
The actual specific equations used by SPICE for the static level 1 model are:

In the linear region:

\[
I_{DS} = KP \frac{W}{L - 2X_{jl}} \left[ (V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2} \right] \left[ 1 + \lambda V_{DS} \right]
\]

In the saturation region:

\[
I_{DSat} = \frac{KP}{2} \frac{W}{L - 2X_{jl}} (V_{GS} - V_{TH})^2 \left[ 1 + \lambda V_{DS} \right]
\]

- \( X_{jl} \) is the lateral diffusion parameter
Threshold voltage

It is important to note that the threshold voltage changes with changes in body-source voltage, $V_{BS}$. SPICE uses the following equation for the threshold voltage:

$$V_{TH} = V_{T0} + \gamma \left( \sqrt{2\phi_p - V_{BS}} - \sqrt{2\phi_p} \right)$$

Where $V_{T0}$ is the threshold voltage when the body-source voltage is zero, $\gamma$ is the body effect parameter and $\phi_p$ is the surface inversion potential.

Note that if the bulk is connected to the source (i.e. the MOSFET is acting as a 3 terminal device, the threshold voltage is always equal to the value $V_{T0}$).

If the bulk voltage is decreased relative to the source, why does the threshold voltage increase?

When would the bulk not be connected to the source?
There is a depletion layer which grows into the accumulation region and thus for a given $V_{GS}$, cuts off the channel. Need to add more $V_{GS}$ to re-establish the channel.

When we have stacked transistors in integrated circuits. If you connected bulk to source on each transistor in an integrated circuit you would end up shorting many points in the circuit to ground.
Complete DC model

- There are the body-source and body-drain diodes
Equations used for the diode models

More simple than the SPICE diode model….

For forward bias on the body-source/body-drain diodes:

\[ I_{BS} = I_{SS} \left[ \exp \left( \frac{V_{BS}}{V_t} \right) - 1 \right] + GMIN \times V_{BS} \]

\[ I_{BD} = I_{SD} \left[ \exp \left( \frac{V_{BD}}{V_t} \right) - 1 \right] + GMIN \times V_{BD} \]

For negative reverse bias on those diodes:

\[ I_{BS} = I_{SS} \frac{V_{BS}}{V_t} + GMIN \times V_{BS} \]

\[ I_{BD} = I_{SD} \frac{V_{BD}}{V_t} + GMIN \times V_{BD} \]
MOSFET body diodes

These reverse bias terms are simply the first terms in a power series expansion of the exponential term. Note that the GMIN convergence resistance is also present.

$I_{SS}$ and $I_{SD}$ are taken to be one constant in SPICE, known as SPICE parameter IS.

- Can sometimes be better to set the body diode parameters to open circuit and add in your own diode model – especially in power electronics
# DC MOSFET parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Channel length</td>
</tr>
<tr>
<td>W</td>
<td>Channel width</td>
</tr>
<tr>
<td>KP (KP)</td>
<td>The transconductance parameter</td>
</tr>
<tr>
<td>VT0 (VT0)</td>
<td>Threshold voltage under zero bias conditions</td>
</tr>
<tr>
<td>GAMMA (γ)</td>
<td>Body effect parameter</td>
</tr>
<tr>
<td>PHI (φp)</td>
<td>Surface inversion potential</td>
</tr>
<tr>
<td>RS (RS)</td>
<td>Source contact resistance</td>
</tr>
<tr>
<td>RD (RD)</td>
<td>Drain contact resistance</td>
</tr>
<tr>
<td>LAMBDA (λ)</td>
<td>Channel length modulation parameter</td>
</tr>
<tr>
<td>XJ (Xjl)</td>
<td>Lateral diffusion parameter</td>
</tr>
<tr>
<td>IS (ISS, ISD)</td>
<td>Reverse saturation current of body-drain/source diodes</td>
</tr>
</tbody>
</table>
Large Signal Transient Model

Again, we need to add some capacitances to the DC model to create the transient model to form the final transient model, as shown below:
Capacitances

Static overlap capacitances between gate and drain ($C_{GB0}$), gate and source ($C_{GS0}$), and gate and bulk ($C_{GB0}$). These are fixed values, and are specified per unit width in SPICE.

**In Saturation:**

\[
C_{GS} = \frac{2}{3} C_{ox} + C_{GS0}W
\]

\[
C_{GD} = C_{GD0}W
\]

No surprise here! In saturation, *i.e.* after pinch-off, the it is assumed that altering the drain voltage does not have any effect on stored charge in the channel and thus the only capacitance between gate and drain is the overlap capacitance.
In the linear/triode region

In this region, the following equations are used:

\[
C_{GS} = C_{ox} \left\{ 1 - \left[ \frac{V_{GS} - V_{DS} - V_{TH}}{2(V_{GS} - V_{TH}) - V_{DS}} \right]^2 \right\} + C_{GS0}W
\]

\[
C_{GD} = C_{ox} \left\{ 1 - \left[ \frac{V_{GS} - V_{TH}}{2(V_{GS} - V_{TH}) - V_{DS}} \right]^2 \right\} + C_{GD0}W
\]

We will not show where these equations come from, but we will make one notable point:

As the device is moved further into the linear region, i.e. $V_{GS}$ becomes large compared to $(V_{DS} - V_{TH})$ then the values of $C_{GS}$ and $C_{GD}$ become close to $C_{ox}/2$ (plus the relevant overlap capacitance).
The body diode capacitances

The capacitances of the body diodes are given by slightly modified expressions for junction capacitances of the diode model:

You are aware of the expression for a pn diode junction capacitance:

\[ C_j = \frac{C_j(0)}{\sqrt{1 - \frac{V}{V_0}}} \]

The MOSFET equation is based on the following slightly modified equation:
The junction capacitance is made up of two components.

- The main component, due to $C_j(0)$ is the normal junction capacitance
- The second parameter is the perimeter junction capacitance of the diffused source.

The diffusion capacitance of the body diodes is not included in the model. Why is this?
The diffusion capacitance is zero in reverse bias – and the MOSFET must be operated with the bulk-drain and bulk-source diodes in reverse bias to stop large bulk currents flowing.

The additional parameters required for specifying the transient model in addition to those required by the DC model are thus:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGD0 (C_{GD0})</td>
<td>Gate drain overlap capacitance per unit width of device</td>
</tr>
<tr>
<td>CGS0 (C_{GS0})</td>
<td>Gate source overlap capacitance per unit width of device</td>
</tr>
<tr>
<td>CJ (C_j)</td>
<td>Zero bias depletion capacitance for body diodes</td>
</tr>
<tr>
<td>CJSW (C_{jsw})</td>
<td>Zero bias depletion perimeter capacitance for body diodes</td>
</tr>
<tr>
<td>TOX (t_{ox})</td>
<td>Oxide thickness (used for calculating (C_{ox}))</td>
</tr>
</tbody>
</table>
Course Summary

• Looked briefly at the algorithms used in SPICE and the need for different models for different types of simulation.

• Need for convergence aids in the Newton-Raphson algorithm

• Diode model – a piece-wise non-linear model that includes breakdown

• BJT model – based on the coupled diode Ebers-Moll model. Very useful as it works in all operating modes for the BJT

• MOSFET model – based on the device equations you already know, but adds in the body diodes