MMIC Components for X- and Ku-band Satellite Systems

M. Gillick, S. Lucyszyn, U. Karacaoglu, I. D. Robertson and A. H. Aghvami

Introduction
This paper describes the design and performance of a range of MMIC components suitable for satellite systems operating in X- and Ku-band. The chips have all been fabricated with the GEC-Marconi (Caswell) standard F20 foundry process, which provides 0.5\(\mu\)m gate-length ion-implanted MESFETs, and through-GaAs via-holes. The circuits described are:- A small-signal amplifier for use as a front-end gain block, a balanced amplifier suitable for a transmitter pre-driver chain, a 1W power amplifier, an analogue phase shifter, a mixer suitable for receivers and up-converters, and finally a VCO suitable for integration into a phase-locked oscillator subsystem.

Small-Signal Amplifier
Fig. 1 shows the complete amplifier circuit including the various matching and biasing networks. High impedance microstrip shorted stubs and series lines are used for the distributed matching elements. Two-finger and four-finger ion-implanted MESFETs are used for the first and second stages respectively. All the matching networks were optimised and synthesised to produce maximum small-signal gain flatness for high amplification and low return loss. Noise figure was not considered as discrete HEMT LNAs are envisaged. Fig. 2 shows a photomicrograph of the fabricated Ku-Band MMIC amplifier with a chip size of 2 x 1 mm. The measured and modelled gain response is shown in Fig. 3. The measured power gain of the amplifier is over 10.5 dB from 13 to 20 GHz. The associated bias was \(V_{dss}=2.5\) volts and \(V_{ds2}=3\) volts at 50% \(I_{dss}\).

CPW Two-Stage Balanced Amplifier
Coplanar waveguide (CPW) has recently been receiving widespread attention for GaAs monolithic microwave integrated circuits (MMICs). The CPW medium is favourable because of source inductance reduction, no via-hole requirements, and its inherent property of minimising line-to-line coupling for high packing-density. Balanced amplifiers are attractive because of their excellent cascadability, high power and good stability, but have the disadvantage of requiring a large chip area due to the coupler's size. Here, the "reduced-size" coplanar waveguide branch-line coupler overcomes this disadvantage. These couplers, employing short high impedance CPW transmission lines and shunt-lumped capacitors occupy less than 25% of the area of the standard branch-line coupler. All parts of the simulations and optimisations were carried out using both the em\textsuperscript{TM} Sonnet software and the GEC-Marconi foundry library models run on Touchstone\textsuperscript{TM} software, and a gain of over 15 dB throughout the band was predicted. Fig. 4 shows a photomicrograph of the fabricated CPW two-stage balanced Ku-Band MMIC amplifier which has a chip size of 2 mm x 1.7 mm. The measured performance shows a good input and output match, along with a gain of 13.7 dB and less than \(\pm 0.2\) dB of ripple over the frequency range 14-16 GHz. From the measured results the calculated gain of 3 cascaded chips is predicted to be 40 dB with a gain variation of less than 1 dB.

Power Amplifier
The recently introduced thin-film microstrip (TFMS) technique has successfully been applied to the miniaturisation of branch-line couplers and a range of novel circuits [1]-[2]. In this technique, multiple metal layers and thin dielectric films are deposited onto the wafer, and the thin dielectric films serve as the 'substrate' for miniature microstrip lines. The increased packing density this allows is considerable, and 50 \(\Omega\) lines have a typical width of only 10 \(\mu\)m.

Communications Research Group  
Dept. of Electronic & Electrical Engineering  
University of London  
Strand, London, UK, WC2R 2LS
In this power amplifier, the thin-film microstrip technique has been extended to realise transmission lines with characteristic impedance as low as 3.5 Ω. For such low impedances, conventional microstrip on thick substrates would be too wide and would suffer frequency limitations due to transverse modes. Hence, in the power amplifier matching networks, conventional microstrip transformers are unrealisable when the device input and output impedances are very low, and so power dividing/combining and cluster matching techniques are usually employed [3]-[4]. Here, TFMS lines overcome this characteristic impedance limit. The main potential drawback with TFMS lines is the increased loss, but in fact the 120 μm line has a measured loss of only 0.7 dB per millimetre at 20 GHz. The amplifier uses the standard GEC-Marconi (Caswell) foundry F20 process, and because the design was on a multi-project wafer it was not possible to use the medium-power foundry process offered by Caswell, nor the high-power R&D process with bath-tub vias. A photomicrograph of the 3 × 2 mm amplifier chip is shown in Fig. 5. Four individual 8 × 175 μm devices were used, connected with a short microstrip feed network. This topology was chosen in order to be able to use standard foundry device models, to ensure equal path lengths to each device, and to ease the thermal problems encountered with a single large device. This FET structure was modelled using small-signal foundry data in order to find the input and output impedances for maximum available gain at 11 GHz. The short impedance transformer technique was then used to match these to 50 Ω. The measured small-signal response is shown in Fig. 6. The gain is over 5.5 dB at the centre frequency of 11.3 GHz. The output match is excellent at better than 25 dB, and the input match is 7 dB at the centre frequency. Spot frequency power measurements were subsequently made using a power meter and a TWT driver amplifier fed from a sweep generator. The output power is just over 1 Watt at 1 dB gain compression, and the power-added efficiency is 18.9%. These results are as expected considering that the low-noise FET had to be used.

**Phase Shifter**

The Cascaded-Match Reflection-Type Phase Shifter (CMRTPS) [5] was recently introduced to give a flat relative phase shift response over a very wide bandwidth. Two single-stage reflection-type phase shifters are cascaded, where the non-linear performance of each stage compliments the other. The topology for the 2-stage CMRTPS is shown in Fig. 7. For an octave bandwidth (6.5 - 13 GHz) realisation, two 4-finger folded Lange couplers were employed, and abrupt junction varactors were realised by connecting together the drain and source terminations of a standard library cell MESFET [6]. The Interdigitated Planar Schottky Varactor Diodes (IPSVD) used in the 1st stage reflection terminations have an effective gate width of 3.6mm, while the 2nd stage reflection terminations have an effective gate width of 1.2mm. For this prototype design, each IPSVD had its own DC probe pad. High value resistors, Rb=6KΩ, were used to limit RF leakage and forward bias current. A microphotograph of the GaAs MMIC, with its dimensions of 3 × 2 mm², is shown in Fig. 8. Fig. 9 shows the relative phase shift frequency response, for various bias levels. At the 10 GHz centre frequency, the relative phase shift varies from 0 to 90°, for a decreasing bias potential from 0 to -7.5V. This 90° level of relative phase shift is achieved with a capacitance ratio of C(0)/C(-7.5V)=4.4, using the F20 process. A maximum peak phase error of +/-3.69° is maintained across the octave bandwidth. At centre frequency, the insertion loss varies from -3.65dB to -2.63dB, for a decreasing bias potential from 0 to -7.5V. A maximum peak amplitude error of +/-0.63dB is maintained across the octave bandwidth. The input return loss performance is approx. 20dB across most of the octave bandwidth. Finally, the measured group delay response was confined within the range of 115ps +/- 13ps, at all bias levels, within the octave bandwidth.

**Mixer**

Balanced mixers have proved to be one of the most difficult circuits to realise properly on MMICs because conventional techniques use non-planar passive baluns or large couplers. A wide variety of possible solutions has been reported, using either FETs or diodes, and with both active and passive baluns. For frequencies up to around 18 GHz, the large size of couplers can be overcome by using lumped-element equivalents [7,8]. More recently, multi-level baluns have been widely reported [9,10] using two overlaid metal layers. FET mixers, and active
baluns and combiners have also received considerable attention, particularly for wideband mixers [11,12]. Passive diode mixers usually lead to high conversion loss and large chip-size. On the other hand, active techniques can result in compact designs with conversion gain, but they are often over-complex, highly sensitive to the operating conditions, and require many DC bias connections. Hence, there is an optimum combination of active and passive techniques, where the simplicity of passive mixers can be blended with the compactness and potential high performance achievable with active techniques.

The technique employed here is to use a lumped-element Wilkinson RF-LO combiner feeding a pair of balanced mixer FETs. The FET pair, one in common-source and one in common-gate configuration, achieves both the active balun and mixing functions. The RF and LO are combined using a lumped-element equivalent of the Wilkinson combiner. The rest of the circuit is simply for DC bias injection and DC blocking. A photomicrograph of the mixer chip is shown in Fig. 10. The chip-size is 1.2 x 1.5 mm, and there is considerable scope for miniaturisation in a second-design. The conversion gain was measured using signal generators and a spectrum analyser. This is found to give very accurate and reliable results. Fig. 11 shows the measured conversion gain frequency response (with a swept LO and a fixed IF of 500 MHz) for 10 dBm of LO power. The mixer has 1dB gain, which is exceptionally flat over the 5 to 12 GHz range, and the mixer inputs are well matched to 50Ω. The port-to-port isolations are also very good: 20 dB of LO/RF-to-IF isolation is achieved. This is a considerable improvement compared with single-ended FET mixers, which often amplify the LO signal. The measured LO to RF isolation, which is governed by the lumped-element Wilkinson combiner, is over 15dB over most of the band, but the centre-frequency of the combiner appears to be too high, and a second pass design could easily achieve higher isolation. Also, a new mixer with an active combiner is currently being designed, which gives more gain and high LO-RF isolation. As well as providing port-to-port isolations, balanced mixers are important for the rejection of unwanted signals. The IF output spectrum, from DC to 2 GHz, shows all unwanted signals are well over 50dB down on the IF. The corrected SSB noise figure is approximately 10 dB between 2 and 14 GHz, which is disappointing but will be improved by the use of the active combiner. The two-tone third-order intercept point is at an IF output level of 10dBm.

VCO
Whilst it has not yet been fabricated and tested, for completeness the VCO chip is included here. Apart from simple TVROs, most systems will require a highly stable oscillator locked to a crystal reference and so the VCO is an important component. The design uses a 4 x 75μm FET, and uses a tuning varactor created from a 6 x 150μm FET. Individual VCOs have been designed to operate at 10, 12, and 14 GHz, and a predicted tuning range of approximately 500 MHz is predicted. Fig. 12 shows the layout of the 10 GHz design, which measures approximately 1.2 x 1.5 mm.

Conclusions
A range of MMIC components suitable for integration into X- and Ku-band satellite systems has been described. For satellite payloads the MMIC approach leads to high reliability and low mass, but cost is not a major criterion. Hence, the designs here could be integrated into compact receiver and transmitter modules as individual functional blocks. However, for applications such as VSAT earth terminals cost is an important criterion and further integration of the functions would be desirable as long as the overall chip area remained at an economical level. With GEC-Marconi’s recent commissioning of a 3" GaAs foundry process, such MMICs are now highly competitive for high volume applications.

Acknowledgements
This work was supported by the Science and Engineering Research Council and by the Defence Research Agency (Electronics Division). M. Gillick is supported by British Aerospace (Space Systems) with an SERC CASE award.
References


Fig. 1. Amplifier circuit diagram

Fig. 2. Photograph of the amplifier chip

Fig. 3. Measured and modelled amplifier gain

Fig. 4. Photograph of the balanced CPW amplifier

Fig. 5. Photograph of the power amplifier chip

Fig. 6. Measured response of the power amplifier
Fig. 7. CMKTPS topology

Fig. 8. Photograph of the phase shifter chip

Fig. 9. Measured phase response of the phase shifter

Fig. 10. Photograph of the mixer chip

Fig. 11. Measured conversion gain of the mixer

Fig. 12. WCD layout