output arrays in such a manner that the PEs of the nth input array \( n = 1, 2, \ldots, L + 1 \) remain sandwiched between

![Diagram of PE-II](image)

\( \text{Fig. 2 Structure of outer layer and PE-II} \)

- Outer layer
- PE-II

In every time step the phase elements \( \phi_i, i = 0, 1, \ldots, L \) are transferred to the adjacent locations towards the right: \( P(\phi) = R' \) and \( P(\phi) = R \).

\( L + 2 \) \(-\)nth PEs of the output arrays. Elements of the nth column \( n = 1, 2, \ldots, L + 1 \) of \( [x(k, n)] \) and \( [z(k, n)] \) (matrices of size \( (L + 1) \times (L + 1) \) obtained according to eqn. 6) are fed serially to the nth input array, in reverse order, staggered by one time step with respect to the corresponding elements of the \( (n+1) \)th columns. One time step is considered as the time required to perform a pair of phase rotations followed by two real additions. In every \( (L + 1) \) time steps each PE-I provides an upward and a downward output, which form the input for the next \( (L + 1) \) time steps, to its neighboring PE-II existing in the outer layers.

**Hardware and throughput considerations:** The proposed architecture requires \( (L + 1)^2 \) PE-II and \( 2L \times 10^2 \) PE-IIs. It computes the first set of 2-D DHTs in \( 4L + 2 \) time steps and successive sets in an interval of \( L + 1 \) time steps. If the scheme of the CORIDC implementation of phase rotation the same as that of Reference 1 is employed in the PEs of the proposed structure, then the hardware requirement of a PE-I and a PE-II would, respectively, \( 2L \times 1 \) and \( 4L \) times and two times that of a PE of Reference 1. As a whole, the proposed structure would require nearly the same amount of hardware as the structure of Reference 1, and the duration of a time step would remain nearly the same for both the structures. However, the present structure would have a throughput rate of \( \sim 2N/\text{time steps} \), and would require a chip area of \( O(N/2 \times N/2L) \), whereas the structure of Reference 1 has a throughput rate of \( \sim [1/(4N^2/4N)] \) and chip area \( O(N^2) \).

**Conclusion:** A recursive algorithm and an efficient architecture have been proposed for computing the 2-D DHT. Besides, the desirable features such as modularity, regular and local connections, and full pipelineability, the proposed structure has a special advantage in that it neither requires any extra hardware nor any extra time for transposition of the intermediate output \( [x(k, n)] \). Transposition is avoided by orthogonal alignment of output arrays with respect to input arrays. Compactness of the structure is achieved by its 3-D nature. Both high throughput as well as compactness have, however, been possible due to the massive parallelism inherent with the proposed algorithm. For a more hardware efficient realisation, a pair of phase rotations of the form \( R'P' \) and \( R'P \), occurring in eqns. 4, 5, and 9, may be performed by a single CORDIC circuit, similar to one suggested in Reference 2 (page 272), where the unnormalised rotations for one phase rotation may be performed simultaneously with the normalisations corresponding to the other.

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**HIGH PERFORMANCE WIDEBAND ANALOGUE TIME SHIFTER**

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**Indexing terms:** Delay lines, Phase shifters

A proof-of-concept analogue reflective-type time shifter is presented for the first time. The measured results for an experimental hybrid realisation, having a centre frequency of 750 MHz, demonstrate a high performance over a 40% bandwidth. The design is totally compatible with monolithic technology and variable for both microwave and millimetre wave applications.

**Introduction** High performance variable time shifters are employed wherever ideal tunable delay lines are required. Examples include: adaptive beam-forming networks for wideband phased array antennas, phased array antennas emulators [3], phase matching networks for radar and ECM subsystem interconnects [2] and building blocks in future analogue signal processing architectures.

Common classes of time shifter, which are compatible with both hybrid microwave integrated circuit (MIC) and monolithic MIC technology, are digital switched-line, analogue loaded-line, and digital reflection-type. The concept of an analogue reflection-type time shifter (RTTS) was only recently introduced [3]. Here, the simulated results of an X-band design, having a maximum relative phase shift of 90°, at a centre frequency of 10 GHz, demonstrated that a high performance was possible over at least a 40% bandwidth. The first measured results for an experimental realisation of this time shifter are presented in this Letter.

**Realisation** The topology of an ideal analogue RTTS simply consists of a 3 dB quadrature directional coupler with identical series L-C tuned circuit reflection terminations connected to its coupled and direct ports and the output taken from the isolated port: this topology has traditionally been associated with reflection-type phase shifters [4]. An analogue RTTS, having a centre frequency of 750 MHz, was realised using microstrip techniques, employing a folded four-finger Lange coupler. The variable capacitors were implemented with mesa-type chip varactor diodes, having abrupt junction characteristics. Each inductor was realised with a single long wire. A photograph of the 0° to 1-inch time shifter is shown in Fig. 1 and the corresponding model is illustrated in Fig. 2.

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Measured results: Conventional on-wafer probing techniques were adopted, in order to avoid any measurement degradation across the 40% bandwidth and at all bias levels. With the model given in Fig. 2, the simulated results predicted all of the measured results, with a high degree of accuracy. This can be seen from the measured and modelled tuning curves, at centre frequency ($f_c = 750$ MHz), shown in Fig. 6. Techniques for encountered with traditional microstrip launchers. To facilitate this, a coplanar waveguide-to-microstrip transition was developed, having low inductance wrap-around grounds. An HP8510B automatic network analyser and a Cascade Summit-9000 analytical probe station were used to perform the measurements.

The measured relative phase shift and group delay performances are shown in Figs. 3 and 4, respectively. The maximum relative phase shift is 90°, at the centre frequency. The group delay responses remain relatively flat across a 40% bandwidth and at all bias levels. The maximum relative group delay shift is 540 ps. Now, a true time shifter is defined by the following expression: $\Delta \tau = (\Delta _{\varphi} S_{11})/\omega$, at all frequencies within its defined bandwidth of operation, where $\Delta \tau$ is the relative group delay shift, $\Delta \varphi$, $S_{11}$, the relative phase shift and $\omega$ the angular frequency. With the analogue RTTS, it is found that this expression holds true within a few percent, across the 40% bandwidth and at all bias levels.

The measured insertion loss and input return loss performances are shown in Fig. 5. The insertion loss is only $-0$ dB at 0.6-dB and the input return loss is better than 14 dB.
improving the tuning linearity and increasing both the maximum relative phase shift (to 180° at centre frequency) and bandwidth have already been suggested [3]. The maximum group delay of 1 ns was obtained with C12 = C4.8 nF = 4-0 pF, which corresponds exactly to the value predicted [3].

The inductor value is approximately 28% higher than the value predicted. Subsequent simulations have shown that the extra inductance is required to compensate for the additional parasitic capacitance to ground.

Conclusions: A proof-of-concept analogue reflection-type time shifter has been realised. Its measured results have demonstrated the potential of this new parametric device. The design is totally compatible with monolithic technology and suitable for both microwave and millimetre wave applications. In addition to its high performance, almost no control power is required, because the varactor diodes are always reverse biased, and only one control wire is required per time shifter. As a result, it is ideally suited for use in the adaptive beam forming networks of very large aperture wideband phased array antennas, intended for future satellite and mobile applications.

References

IMPROVING THE PERFORMANCE OF THE QUADTREE-BASED IMAGE APPROXIMATION VIA THE GENERALISED DCT

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Indexing terms: Image coding, Transforms

An algorithm is presented to improve the performance of the quadtree-based image approximation using the generalised discrete cosine transform. The results show that the number of coefficients for the approximation can be further reduced remarkably while the approximation error increases only slightly.

Introduction: The transform image coding technique has been proved to be very efficient when the image data are strongly correlated in texture. The purpose of the orthogonal transform used in image coding is to convert the statistically-dependent samples of the data into a set of 'more independent' coefficients to condense the major part of the information into a small percentage of the transform domain components. The most popular transform is the discrete cosine transform (DCT) because its performance is close to that of the Karhunen-Loeve transform which is known as being optimal assuming the image to be statistically stationary. Unfortunately, the assumption of stationarity is not true for almost all types of real-world images; thus variable block size algorithms are created which change the block size to adapt to the local activities of the image. Among them, quadtree-based DCT coding has proved to be very efficient [1-4].

The quadtree-based DCT coding algorithm is an adaptive technique in which the adaptivity is achieved by changing the block size according to the activities of the block. In this Letter, we show that the performance can be much improved by merging those quadtree blocks having similar activities without greatly increasing the mean-square errors, via the generalised DCT presented in the Reference below.$^*$

The number of blocks is much reduced, thus a lower coding rate can be achieved.

Quadtree-based DCT image approximation: A quadtree is a hierarchical data structure in which each node generates four subnodes. In the quadtree-based image approximation algorithm, the image block may be split into four sub-blocks of the same size based on a criterion to check if the split should take place.

The use of the DCT is to compact the energy of the block into a small percentage of the transform components. Discarding those small energy components results in a relatively small error. The image block can be approximated by much fewer coefficients through the discarding process. The splitting criterion is carried out by first measuring the error and then comparing it with a given threshold as:

\[
\text{error} > \text{threshold} \quad \text{then split;}
\]
\[
\text{else do not split.}
\]

To avoid the size of each region becoming too large, the error measure is defined as

\[
\text{error} = \frac{1}{N_x N_y} \sum_{i,j} \left( |X_{ij} - \bar{X}_{ij}|^2 \right)
\]

where \( S \) is the region, \( N_x \) is the number of elements in \( S \) and \( \bar{X} \) is the approximation for \( X \). The purpose of the weighting is to avoid the size of each segmented region becoming too large causing blocking effects, and to reduce the number of the small regions.

Fig. 1 shows the image for an example of quadtree-based DCT approximation. The mean square error is shown as the

\[887\]

\[156\]

Fig. 1 Quadtree-based DCT approximation