Noise in nanometric s-Si MOSFET for low-power applications

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Abstract. This paper reports on the influence of the gate length reduction on the noise performance of strained-Si surface channel MOSFETs for very low power applications. When the gate length is reduced from 100nm to 20nm an increase of the current gain is achieved that nearly doubles the cut-off frequency of the transistor. This is counterbalanced by a deterioration of the noise figure and the noise resistance of the device for low values of the drain current.

Keywords: Hydrodynamic Model, SiGe, MOSFET, Noise, Fluctuations

PACS: 72.70.+m, 73.50.Td

INTRODUCTION

MOSFET production reached sub-100 nm dimensions in 2001 with Intel shipping 60-nm transistors in the 130-nm bulk CMOS technology node. Recently, the semiconductor industry leaders have shifted the production to the 90-nm node involving even shorter gate lengths. Nevertheless, there is a general consensus in contemplating bulk CMOS as being impractical for future nodes due to heating originated from leakage currents. The introduction of new alternative technologies to bulk CMOS is a pressing issue. The ones based on the system Si/SiGe left the status of promising technology earned in the 90s to enter the production phase in Intel in 90-nm logic circuits. A considerable number of research papers have been published on the possible improvements of n-channel FETs with strained Si channels, both using a buried channel (s-Si MODFET) and a surface channel configuration (s-Si MOSFET). Those technologies have a huge potential for analog and low-power applications. So far minimum noise figures as low as 0.4dB at 2.5GHz and cut-off frequencies (fT) in excess of 70GHz at 300K have been reported in s-Si MODFETs. Recently, we reported encouraging results on the performance of Si/SiGe devices operating in low-power regime when compared with state of the art bulk CMOSs.

MODEL AND SIMULATED DEVICES

In this paper we report on the calculated noise properties of sub-100nm s-Si MOSFET operating in ultra low-power conditions at room temperature. To this aim
we kept the drain to source bias at $V_{DS}=50mV$ and the gate to source bias ($V_{GS}$) was varied in a voltage range around the threshold voltage ($V_{th}$). The vertical lay-out of the simulated devices from top to down is: a degenerately doped polysilicon gate, a 6 nm-thick SiO2 oxide layer, an 8nm-thick quantum well (QW), a 200nm-thick Si$_{0.7}$Ge$_{0.3}$ set back layer (SBL) grown on top of the graded virtual substrate (VS) and a conventional high-resistivity p-Si wafer. The QW, SBL and VS regions are nominally undoped and the source/drain contacts are assumed self-aligned to the polysilicon gate. Three gate lengths ($L_g$) have been considered: 100nm (T1), 50 nm (T2) and 20 nm (T3). Two-dimensional simulations have been performed using Synopsys’ Taurus/Medici$^\text{TM}$ implementing an energy balance transport model$^6$. In the simulations, impurity de-ionization, Fermi-Dirac statistics and mobility degradation due to both longitudinal and transverse electric field, have been taken into account. The oxide-channel interface and the oxide itself were assumed to be free of traps and fixed charges. Nevertheless, the degradation of the low-field mobility at the channel surface was considered through the use of the Roldan’s model$^5$. For the simulation of the noise in the MOSFETs we adopted the Impedance Field Method with Langevin stochastic noise sources. We assumed that only thermal (diffusive) noise exists and other noise sources originating from processes such as recombination were not considered in this study.

**STEADY-STATE AND DYNAMIC RESULTS**

Figure 1 shows the transfer and the transconductance ($g_m$) characteristics of T1, T2 and T3. There is a noticeable $V_{th}$ roll-off and a degradation of the subthreshold slope (100mV/decade in T1 to over 200mV/decade in T3) as $L_g$ decreases. All the magnitudes presented hereafter are normalized assuming a device’s width of 1$\mu$m in the non simulated direction.

**FIGURE 1.** $I_{DS}$-$V_{GS}$ characteristics (left) and transconductance (right) of T1, T2 and T3 ($V_{DS}=50mV$).

The modest increase of the transconductance when shrinking the gate length is a result of several factors: the increased difficulty to keep an adequate carrier confinement in the QW, the mobility degradation due to stronger electric fields in the channel and the fact that the oxide thickness is not scaled down accordingly to the $L_g$ reduction. Nevertheless, maintaining the oxide thickness pays back in terms of the cut-
off frequency as can be seen in Fig. 3. As $L_g$ is reduced from 100nm (T1) to 20nm (T3) the maximum of $f_T$ is doubled. This enhancement, not found in $g_m$, is essentially supported by the gate capacitance reduction.

**FIGURE 2.** Total gate capacitance (left) and cut-off frequency (right) of the simulated transistors.

**NOISE ANALYSIS**

In this section we present some noise parameters (namely the noise figure and the noise resistance) that are useful to evaluate the noise performance of the device for analog applications. In this study the $V_{GS}$ sweep is limited to a few hundreds of mV around $V_{th}$ in order to maintain the drain current at values sufficiently low to allow for low-power operation ($V_{DS}$ is being kept at 50mV).

In Fig. 3 we present the noise figure (NF) for the devices under study at a frequency of 1GHz. The minimum value of the NF shifts towards lower values of $V_{GS}$ as $L_g$ decreases (by -60mV as $L_g$ is reduced from 100 to 20nm, Fig. 3, left) at a slower pace than the $V_{th}$ roll-off (by -100mV for the same variation of $L_g$). As a direct consequence of this the NF steadily grows when the gate length shrinks for all drain current levels under 1μA (Fig. 3, right).

The above behaviour of the noise figure must be understood as a consequence of the combination of the significant resistances across both the intrinsic device and the
implanted source and drain regions. Bearing that in mind, we calculated the minimum noise figure ($N_{\text{Fmin}}$) at the same frequency (Fig. 4, left). Again the shorter gate length transistor (T3) exhibit the largest noise value at very low drain currents. Only for drain current values in excess of 0.8µA does T3 exhibit the best performance in terms of $N_{\text{Fmin}}$. Of course, lower values of $N_{\text{Fmin}}$ can be achieved if the source/drain access regions are optimized. In the simulations we maintained the same implantation profile for all devices T1, T2 and T3.

![FIGURE 4. Minimum Noise Figure (left) and noise resistance (right) of the simulated transistors plotted against the drain current at 1GHz.](image)

Fig. 4 (right) shows the calculated noise resistance ($R_n$) at 1GHz. The noise results closely follow the behaviour of NF in Fig. 3 (right). This points out that a significant degradation of the noise performance will follow any gate length reduction when devices operate at very low drain current levels. These effects could be partly mitigated through a careful redesign of the lateral structure.

**ACKNOWLEDGMENTS**

This work was founded by EPSRC award N. GR/N65844/01, by MCYT/FEDER (TIC2001-1757) and Junta de Castilla y León (SA066/02).

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